SIDDHARTH INSTITUTE OF ENGINEERING AND TECHNOLOGY :: PUTTUR
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QUESTION BANK

Subject with Code : Advanced Computer Architecture (16EC5503)

Course & Branch: M.Tech – (VLSI,DECS) **Year & Sem:** I-M.Tech & I-Sem

UNIT –I

1. a) Discuss the technology trends of computers. [5M]

   b) Explain the methods of system design cost measuring. [5M]

2. a) Explain the concept of speed of hardware and its cost. [5M]

   b) Write a short note on fundamentals of a computer design. Explain in detail the quantitative principles of computer design [5M]

3. a) Explain how the performance is measured for system. [5M]

   b) List the different programs for performance calculations [5M]

4. a) Explain how Amdahl's law is useful for measurement of improved performance of computer systems [5M]

   b) Discuss the CPU performance equation [5M]

5. a) Classify the instruction set architecture [2M]

   b) Explain different instruction set architectures. [8M]

6. a) What is addressing mode [2M]

   b) Explain different addressing modes [8M]

7. a) Which type of addressing mode is used for signal processing. [5M]

   b) List different types of operands [5M]

8. a) Give different sizes of operands used in processors. [2M]

   b) Explain various operations in the instruction set. [8M]

9. a) Discuss different control flow instructions. [5M]

   b) How the encoding of an instruction is done in processors. [5M]

10. a) Distinguish between RISC and CISC instruction set [5M]

b) Explain the roll of compilers. [5M]

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UNIT-II

1. a) What is pipelining and parallel processing. [5M]

b) Explain instruction level parallelism. [5M]

2. a) List different data dependences [2M]

b) Explain data hazards [8M]

3. Explain data hazards overcoming with dynamic scheduling with suitable example [10M]

4. a) Give the details of different control dependences. [5M]

b) Explain different branch cost reduction schemes. [5M]

5. a) Explain how to achieve more ILP using multiple issues. [5M]

b) List different limitations of ILP. [5M]

6. a) Explain hardware based speculation. [5M]

b) Give the details of static branch prediction [5M]

7. Explain different compiler techniques for exposing ILP. [10M]

8. a) Discuss performance issues and applications of pipelines [5M]

b) Write short notes on VLIW approach. [5M]

9. Explain different hardware support for achieving more parallelism at compile time [10M]

10. a) Explain briefly about detecting and exhausting loop level parallism. [5M]

b) Differentiate hardware versus software approach of ILP. [5M]

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UNIT-III

1. a) What is cache memory. [2M]

   b) Draw and discuss typical memory hierarchy structure in computers. [8M]

2. a) Define cache miss and cache hit. [2M]

   b) Give the details of cache performance equation. [8M]

3. a) What are the two methods of writing to cache. [2M]

   b) How the memory blocks are filed in cache memory from main memory. [8M]

4. a) Explain how to reduce the miss rate in cache memories. [5M]

   b) What are the problems associated with multi cache? Suggest suitable solutions [5M]

5. a) What is miss penalty [2M]

   b) Explain the different ways of reducing cache miss penalty. [8M]

6. a) Give the reasons why cache coherence is an accepted requirement in small scale multiprocessors. [5M]

   b) Draw the state transition diagram for an individual cache block in a directory based system.[5M]

.7. a) Explain the concept of virtual memory. [5M]

   b) What is virtual address and physical address. [5M]

8. a) What is the function of TLB. [2M]

   b) Explain the process of protection of virtual memory is achieved. [8M]

9. a) How to evaluate the performance of symmetric shared memory multiprocessors. [2M]

   b) Explain symmetric and shred memory architectures. [8M]

10. a) Explain hardware primitives for synchronization. [5M]

    b) Discuss any two multi – threaded models. [5M]

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